B.E. (Electronics Engineering / Elect. & Telecommunication / Elect. & Communication Engineering) Seventh Semester (C.B.S.)

Advanced Digital System Design

P. Pages : 2 **NRJ/KW/17/4585/4593**

Time : Three Hours * 0 4 4 6 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) What are the advantages of VHDL over other conventional programming Languages? **5**

b) Explain in detail with suitable- flow chart about the development of digital system with VHDL. **8**

OR

2. a) Explain the different design units used in VHDL with their syntax. **8**

b) Discuss various levels of abstractions in VHDL. **5**

3. a) Explain various data types supported by VHDL. **8**

b) Write a VHDL code for a 3:8 decoder using a selected signal assignment statement. **6**

OR

4. a) What are different data objects used in VHDL? Explain with suitable example. **7**

b) Write a VHDL code for BCD to seven segment decoder. **7**

5. a) What is subprogram? Explain 'Function' and 'procedure' with their syntax. **8**

b) Write a test bench for 8:1 MUX. **5**

OR

6. a) Write the structural description of 16:1 MUX using 4:1 MUX using VHDL. **7**

b) Write a VHDL code for 'Byte Adder' circuit using GENERATE statement. **6**

7. a) Write the difference between Moore and Mealy circuits. **3**

b) Design a sequence detector for 0101 with mealy state machine and implement it with D flip flops and write VHDL code for the same. **10**

OR

8. Design a fundamental mode sequential circuit with two inputs X_1 and X_2 and one output Z. The output Z = 1 if both inputs X_1 and X_2 are equal to 1, but only if input X_1 becomes one before input X_2. **13**

9. a) Explain the concept of synthesis? Explain step by step process of synthesis. **6**

b) Write a short note on 'Power Analysis in FPGA based system'. **7**

OR

10. Write short note on **any two.** **13**

a) Partitioning for synthesis.

b) Pipelining in VHDL.

c) Optimization of Arithmetic Expression.

11. a) A combinational circuit is defined by the function: $F_1(A, B, C) = \sum m\ (3, 5, 6, 7)$. $F_2(A, B, C) = \sum m(0, 2, 4, 7)$. Implement the circuit with a PLA having 3 inputs four product terms and two outputs. **7**

b) Explain the architecture of FPGA with neat diagram. **7**

OR

12. a) Design 4-bit barrel shifter and write VHDL code for it. **7**

b) Write VHDL code for 4-bit ALU. **7**

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