

VKR/KS/13/3270/3362

Faculty of Engineering & Technology
Eighth Semester B.E. (Electronics)/E.D.T. Examination
DIGITAL SYSTEM DESIGN
Sections—A & B

Time : Three Hours] [Maximum Marks : 80

INSTRUCTIONS TO CANDIDATES

- (1) All questions carry marks as indicated.
- (2) Answer **THREE** questions from Section A and **THREE** questions from Section B.
- (3) Due credit will be given to neatness and adequate dimensions.
- (4) Assume suitable data wherever necessary.

SECTION—A

1. (a) Explain data objects in VHDL. 7
(b) Explain Top down and bottom up approach for digital system design in VHDL. 7
2. (a) Write a VHDL code for a four bit barrel shifter. 6
(b) Write a VHDL code for 8 bit full adder using generate statement. 7

3. (a) Explain following attributes in VHDL :
 (i) VALUE
 (ii) FUNCTION. 6
- (b) Write a VHDL code for 4 to 16 binary decoder using generate statement. 7
4. (a) Explain configuration and package declaration with one example of each. 6
- (b) Write a VHDL code for BCD to seven segment decoder. 7
5. (a) Design a 16 : 1 MUX using 4 : 1 MUX. Also write VHDL code using structural style. 7
- (b) Write a test bench to test the 16 : 1 MUX design. 6

SECTION—B

6. (a) Write a VHDL code for 4 bit up down counter with a synchronous reset. 6
- (b) Explain Linear Feedback shift register. 7
7. Write a VHDL code for sequence detector to detect the sequence 0110 using Moore FSM (overlapping is permitted). Also write a test bench for it. 13
8. A fundamental mode circuit has two inputs X_1 and X_0 and single output Z when $X_1X_0 = 00$, $Z = 0$. To make

$Z = 1$ we start with $X_1X_0 = 00$ and first change X_0 to 1 and next change X_1 to 1. To return Z to $Z = '0'$ we must return to $X_1X_0 = '00'$, the order at return being no consequence. Design the circuit using JK flip flop. 14

9. (a) Explain static and dynamic Hazards in digital circuit. 7
- (b) Explain races and cycles in digital circuits. 6
10. Write short notes on :—
 (i) Architecture of Xilinx KPGA
 (ii) PLA
 (iii) ROM. 13