B.E. (Elect. & Telecommunication / Elect. & Communication Engineering)
Eighth Semester (C.B.S.)

Elective-III : CMOS VLSI Design

P. Pages : 2 **NRJ/KW/17/4708**

Time : Three Hours * 0 2 6 6 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Explain the operation of pMOS enhancement transistor. **7**

b) Derive the expression for gm in linear and saturation region for small signal model of MOS transistor. **6**

OR

2. a) Explain body effect and state its impact on overall threshold voltage. **6**

b) Calculate the native threshold voltage for an n-transistor at 300ºK for a process with a Si substrate with $N_A = 1.80 \times 10^{16}$, a SiO_2 gate oxide with thickness $200\,\text{Å}$. (Assume $\phi_{ms} = -0.9\,V$, $Q_{fc} = 0$). **7**

3. a) Explain the operation of CMOS inverter and draw DC transfer characteristic. Derive the expression for V_{out} in the region D of operation. **8**

b) Explain the operation of BiCOMS inverter. **6**

OR

4. a) Calculate the noise margin for a CMOS inverter operating at 3.3 V with $V_{th} = 0.7\,V$, $V_{tp} = -0.7\,V$, $\beta_n = \beta_p$. What would you do to the transistor characteristics to improve the noise margin? **8**

b) Design 4 : 1 multiplexer using transmission gate. **6**

5. a) Design CMOS logic gates for the following functions : **10**

i) $Z = \overline{((A \cdot B \cdot C) + D)}$ ii) $\overline{((A \cdot B) + C) \cdot D)}$

iii) $Z = \overline{((A \cdot B) + C \cdot (A + B))}$ iv) $\overline{((A \cdot B) + (C \cdot D))}$

b) Implement 2 : 1 multiplexer using CMOS Logic gates. **3**

OR

6. a) Explain SRAM & DRAM. **6**

b) Design a CMOS positive level sensitive D latch. **7**

7. a) Describe static power dissipation, short circuit dissipation & hence total power dissipation. **7**

b) Explain capacitance estimation of MOS device indicating accumulation, depletion, inversion & explain its variation as a function of Vgs. **7**

OR

8. a) Write short note on charge sharing. **6**

b) Derive the expression for rise time, fall time and delay time of a CMOS inverter. **8**

9. a) Draw the stick layout for the function $Z = \overline{A + BC + DE}$ using CMOS logic. Also draw Euler's graph and find the Euler's path. **7**

b) What is Latch - up? State methods to prevent Latch - up. **6**

OR

10. a) State various clocking strategies. **7**

b) Implement function $f = \overline{A \cdot B + C}$ using **6**

i) Dynamic Logic

ii) Domino Logic

11. a) Explain Fault model used in VLSI & Explain types of Faults. **7**

b) Explain need for Design for testability. **6**

OR

12. a) Explain Built In Self Test (BIST). **6**

b) Explain Partial Scan & Boundary Scan. **7**

****