Faculty of Engineering & Technology

Eighth Semester B.E. (Industrial Electronics)

Examination

DESIGN OF ELECTRONIC CIRCUITS

Sections—A & B

Time : 3 Hours] [Maximum Marks : 80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Answer **TWO** questions from Section A and **TWO** questions from Section B.

(3) Due credit will be given to neatness and adequate dimensions.

(4) Assume suitable data wherever necessary.

(5) Illustrate your answers wherever necessary with the help of neat sketches.

(6) Use of Non-programmable calculator is permitted.

SECTION—A

1. (a) Design an unregulated DC power supply with capacitor filter arrangement is used to supply 400 mA current to a circuit operating at 12 V DC. The ckt. can tolerate 3 V peak to peak ripple voltage. Assume supply frequency 50 Hz. 8

(b) Design a step-up type SMPS to provide V_o = 25 V at 1.5 A. The unregulated input is 12 V. Time period of switching regulator is 40 μsec. The ON voltage of diode and transistor is 1 V each. The transistor used as switching time 1.2 μ sec. $I_{Coff.}$ = 10 mA. If the output ripple is to be limited to 300 mV (P—P) and resistor is 35 mΩ effective series resistance, find the value of L and C. Assume $V_{ref.}$ = 1.4 V. 12

2. (a) Design a Series Voltage Regulator to give V_o = 12 V at 350 mA. If V_i = 26 V ± 15% at no load, r_o = 3 Ω, h_{fe1} = 40, h_{le2} = 100, find out the values of S_v and R_o. 12

(b) Write a short note on class-C tuned amplifier with neat sketch. 8

3. Design Bootstrapped emitter follower ckt. to give V_o = 0.3 V peak if source voltage V_s = 0.5 V peak. Assume V_{CC} = 12 V, I_C = 0.7 mA. Capacitively coupled R_L = 3 K. Transistor used has h_{fe} = 100. Source resistance of signal generator is 60 K. 20

4. (a) Design a 4 bit DAC using binary weighted resistance and reference voltage of 10 V. Find the output voltage if the binary input is 0011. 12

(b) Write a short note on Sample and Hold Circuit. 8

SECTION—B

5. (a) Differentiate between Active and Passive Filters. 6

(b) Design a Butterworth filter which will give 2 dB attenuation at 1 kHz and 20 dB at 8 kHz. 14

6. Derive the expression for frequency of oscillation and figure of merit for Colpitt's oscillator. 20

7. (a) Differentiate between Combinational Logic and Sequential Logic. 5

(b) Design a ckt. using PLA so as to implement BCD to excess 3 code conversion. 15

8. Write short notes on (any **TWO**) :—

(i) Chopper using transistors

(ii) Algorithmic State machine

(iii) Voltage controlled oscillator (VCO)

(iv) Converter for DC motors. 20