B.E. (Computer Engineering) Semester Third (C.B.S.)

Digital Electronics Paper - II

P. Pages : 2 **KNT/KW/16/7248**

Time : Three Hours * 0 9 2 3 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Assume suitable data whenever necessary.
9. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Convert the following numbers as directed. **8**

i) $(27\cdot125)_{10} = (?)_2 = (?)_{16}$

ii) $(1001\cdot0101)_2 = (?)_{\text{Graycode}}$

iii) $(476\cdot25)_{10} = (?)_{BCD} = (?)_{EX-3}$

iv) $(DEF\cdot AB)_{16} = (?)_2 = (?)_{10}$

b) Explain how a transistor is used as a switch? **3**

c) State and prove Demorgan's law. **3**

OR

2. a) Prove using Boolean Algebra. **6**

i) $A + \overline{A}B + A\overline{B} = A + B$

ii) $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = AB + BC + AC$

b) Define following terms with respect to logic families. **4**

i) Propagation Delay.
ii) Fan out
iii) Fan In
iv) Noise Margin

c) Convert following expression to standard POS form **4**

$f(A,B,C,D) = (A+B+C)+(A+\overline{B}+C)+(A+B)+(\overline{A}+D)$

3. a) Design 2 bit comparator circuit using logic gates. **7**

b) Implement 1:32 Demultiplexer using 1:8 Demux and 1:4 Demux. **6**

OR

4. a) Realize a 5x32 Decoder using 3x8 and 2x4 decoder. **6**

b) Write short note on four input priority Encoder. **7**

5. a) Implement full adder using one 4:1 MUX and NAND Gate. **5**

b) Simplify using K-map. **8**

i) $f(A,B,C,D)=\sum m(0,1,2,3,5,7,8,9,10,13,14)$

ii) $f(W,X,Y,Z)=\pi M(0,1,4,5,9,11,14,15)+d(6,10,13)$

OR

6. a) Minimize the following Boolean equation using K-map and implement the circuit using NAND Gate. $f(A,B,C,D,E)=\sum m(1,4,6,10,20,22,24,26)+d(0,11,16,17)$ **8**

b) Implement the function using K-map. $f(A,B,C,D)=\overline{B}\,\overline{D}+\overline{A}\,\overline{C}+\overline{A}\,B\,\overline{D}$ **5**

7. a) Explain the working of J-K flip-flop. Design the J-K flip-flop using NAND gate only. What is Race-around condition & how it can be eliminated? **9**

b) Explain different methods used for triggering flip-flop. **4**

OR

8. a) Convert. **8**

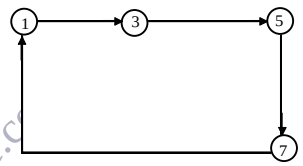
i) JK flip-flop to S-R flip-flop

ii) T – flip-flop to J-K flip-flop

b) Explain the concept of preset & clear in flip-flops. **5**

9. a) Compare combinational and sequential circuits. **2**

b) Design a Lock-free counter for the following state diagram using J-K flip-flop. **8**



c) Design a MOD-6 asynchronous counter. **4**

OR

10. a) Draw and explain four bit Ripple Up-Down counter. **7**

b) Design a 3-bit synchronous Gray coded counter using D- flip-flop. **7**

11. a) Design full subtractor using 2 half subtractors & one OR gate. **6**

b) Design BCD Adder circuit. **7**

OR

12. a) Write short note on the following.

i) ALU **4**

ii) Parallel adders. **4**

iii) Multivibrators **5**

****