

B.E. (Elect. & Telecommunication / Elect. & Communication Engineering)
Seventh Semester (C.B.S.)

Elective - I : VLSI Signal Processing

P. Pages : 3

Time : Three Hours



NRJ/KW/17/4597

Max. Marks : 80

- Notes :
1. All questions carry marks as indicated.
 2. Solve Question 1 OR Questions No. 2.
 3. Solve Question 3 OR Questions No. 4.
 4. Solve Question 5 OR Questions No. 6.
 5. Solve Question 7 OR Questions No. 8.
 6. Solve Question 9 OR Questions No. 10.
 7. Solve Question 11 OR Questions No. 12.
 8. Due credit will be given to neatness and adequate dimensions.
 9. Assume suitable data whenever necessary.
 10. Illustrate your answers whenever necessary with the help of neat sketches.
 11. Use of non programmable calculator is permitted.

1. a) Consider a direct form implementation of the FIR filter,
 $y(n) = a \cdot x(n) + b \cdot x(n-1) + c \cdot x(n-2]$
 Explain how critical path can be reduced with the help of pipelined architecture. **8**
- b) In the signal flow graph (SFG) shown in fig. 1 the computation time for each node is assumed to be 1 u.t. **6**
 - a) Calculate the critical path computation time.
 - b) The critical path has been reduced to 2 u.t. by inserting 3 extra delay. Is this a valid pipelining? If not obtain an appropriate pipelined circuit with critical path of 2 u.t.

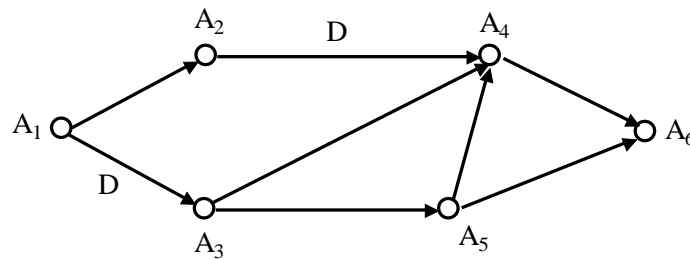


Fig. 1

OR

2. a) Explain how pipelining can be used for reducing power consumption. **7**
- b) Explain how parallel processing can be used for reducing power consumption. **7**
3. a) Demonstrate how shortest path algorithms can be used to solve a system of $M = 5$ inequalities. **6**

$$\begin{aligned} r_1 - r_2 &\leq 0 \\ r_3 - r_1 &\leq 5 \\ r_4 - r_1 &\leq 4 \\ r_4 - r_3 &\leq -1 \\ r_3 - r_2 &\leq 2 \end{aligned}$$

b) What is Retiming? Explain properties of Retiming.

7

OR

4. For a given DFG obtain retiming solution for desired clock period $C = 3$ also draw retiming DFG. (fig. 3)

13

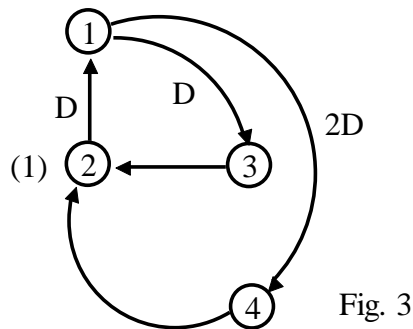


Fig. 3

5. a) Design unfolded architecture with $J = 3$ for the given DFG. (fig. 4). J: unfolding factor

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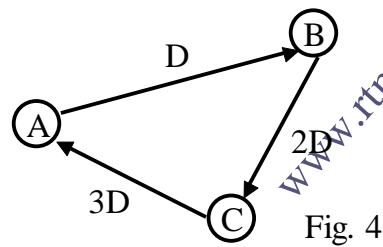


Fig. 4

b) Give the properties of unfolding.

6

OR

6. a) Explain word level and Bit level processing.

6

- b) Consider a DSP program that produces $y(n) = a \cdot x(n) + b \cdot x(n-4) + c \cdot x(n-6)$ shown in figure 5 with $J = 3$.

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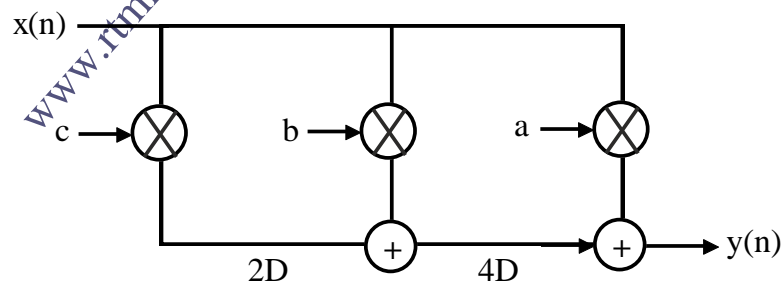


Figure 5

find, 1) Unfolded architecture

2) Parallel processing architecture.

7. a) Fold the retimed DFG of fig 6 using the folding set given as $S_1 = \{4, 2, 3, 1\}$ and $S_2 = \{5, 8, 6, 7\}$.

8

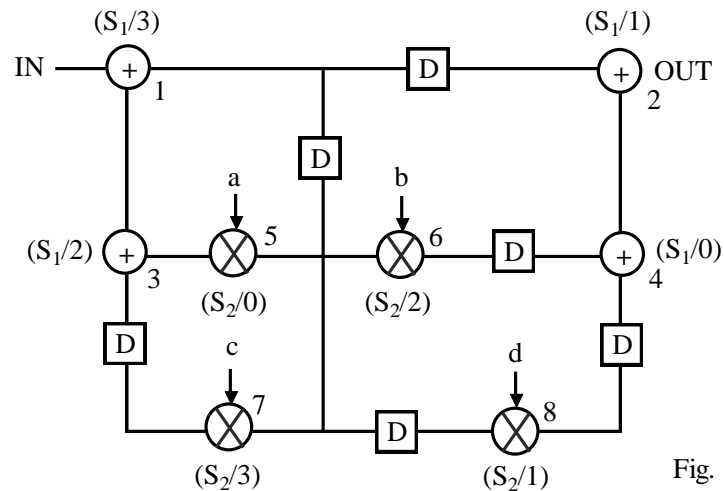


Fig. 6

Assume following data :

Addition and multiplication require 1 and 2 u.t. respectively 1 - stage pipelined address and 2 stage pipelined multipliers are available. Folding factor is $N = 4$. Each operator is clocked with clock period 1 u.t. The folding set are given as

$S_1 = \{4, 2, 3, 1\}$ and $S_2 = \{5, 8, 6, 7\}$.

- b) Explain folding transformation.

6

OR

8. Consider a DSP program that perform transpose operation of 3×3 matrix shown in fig.

14

$$\text{The Matrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$$

find,

- 1) Lifetime analysis
- 2) Data allocation using forward backward register allocation.
- 3) Register minimization of folded architecture.

9. a) Construct a 2×2 convolution algorithm using cook toom algorithm with $\beta = 0, \pm 1$.

10

- b) Write steps for solving modified cook toom algorithm.

3

OR

10. a) Consider a 2×3 linear convolution, construct an efficient realization using winograd algorithm with,

10

$$m(p) = p(p-1)(p^2+1)$$

- b) Explain modified winograd algorithm in short.

3

11. Explain in detail,

13

- a) Fast Convolution
- b) Cyclic Convolution

OR

12. a) Construct a 4×4 line as convolution algorithm using 2×2 short convolution.

8

- b) Define Iterated convolution & write its algorithm.

5
