## NTK/KW/15/7545

9. Construct a $2 \times 3$ convolution algorithm using winograd algorithm with $\mathrm{M}(\mathrm{P})=\mathrm{P}(\mathrm{P}-1)\left(\mathrm{P}^{2}+1\right)$. 14

## OR

10. (a) Explain the steps in modified Cook Toom algorithm.
(b) Constract a $2 \times 2$ convolution algorithm using Cook-Toom algorithm with $\mathrm{b}=0, \pm 1 . \quad 9$
11. (a) Explain steps of iterated convolution algorithm. 3
(b) Construct a $4 \times 4$ linear convolution algorithm using 2 $\times 2$ short convolution.

OR
12. Construct a $4 \times 4$ cyclic convolution algorithm using CRT with

$$
m(P)=P^{4}-1=(P-1)(P+1)\left(P^{2}+1\right) \cdot 13
$$

## Faculty of Engineering \& Technology

 Seventh Semester B.E. (EC/ET) (C.B.S.) Examination ELECTIVE-I : VLSI SIGNAL PROCESSINGTime-Three Hours]
[Maximum Marks-80

## INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.
(2) Solve Question No. 1 OR Question No. 2.
(3) Solve Question No. 3 OR Question No. 4.
(4) Solve Question No. 5 OR Question No. 6.
(5) Solve Question No. 7 OR Question No. 8.
(6) Solve Question No. 9 OR Question No. 10.
(7) Solve Question No. 11 OR Question No. 12.
(8) Due credit will be given to neatness and adequate dimensions.
(9) Assume suitable data wherever necessary.
(10) Illustrate your answers wherever necessary with the help of neat sketches.
(11) Use of non programmable calculator is permitted.

1. (a) Explain the structure of direct form FIR filter \& data broadcast form FIR filter. Show that the data broadcast form can achieve a faster clock rate.
(b) It is necessary to reduce the power consumption of a system by at least 5 times using pipelining. For the threshold voltage of 0.4 V and initial supply voltage of 5 V , at what level should the system be pipelined? What is the supply voltage of the pipelined system ?

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## OR

2. (a) How pipelining can be used to reduce power consumption? Explain in detail.
(b) Show that parallel processing reduces the power consumption of a system.
3. (a) What is retiming ? Explain the method of retiming which uses cutest in combination of slowdown. 6
(b) Explain properties of retiming with example.

## OR

4. Draw a constraint graph and use it to determine if the following system of inequalities has a solution and find a solution if one exists using Bellman-Ford algorithm. 13

$$
\begin{aligned}
& \mathrm{r}_{1}-\mathrm{r}_{2} \leq 0 \\
& \mathrm{r}_{3}-\mathrm{r}_{1} \leq 5 \\
& \mathrm{r}_{4}-\mathrm{r}_{1} \leq 4 \\
& \mathrm{r}_{4}-\mathrm{r}_{3} \leq-1 \\
& \mathrm{r}_{3}-\mathrm{r}_{2} \leq 2
\end{aligned}
$$

5. (a) Show that unfolding preserves the total no. of delays.

6
(b) Perform Unfolding with unfolding factor $\mathrm{J}=3$ for the given Figure 1.

7


## OR

6. Describe how to design parallel processing architectures using unfolding.
7. (a) Explain the folding algorithm. 6
(b) Explain life-time analysis for register minimisation.

## OR

8. Consider a DSP program that performs transpose operation of $3 \times 3$ matrix shown below.

Find :
(1) Life time analysis
(2) Data allocation using forward backward
(3) Register minimization.

The matrix is :

$$
\left[\begin{array}{lll}
\mathrm{a} & \mathrm{~b} & \mathrm{c} \\
\mathrm{~d} & \mathrm{e} & \mathrm{f} \\
\mathrm{~g} & \mathrm{~h} & \mathrm{i}
\end{array}\right]
$$

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