B.E. (Electronics Engineering / Elect.& Telecommunication / Elect.& Communication Engineering)
Seventh Semester (C.B.S.)

DSP Processor & Architecture

P. Pages : 2 **NRT/KS/19/3527/3535**

Time : Three Hours * 0 2 4 0 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Illustrate your answers whenever necessary with the help of neat sketches.
10. Use of non programmable calculator is permitted.

1. a) Explain the difference between von-Neumann and Harvard architecture for the computer. Which architecture is preferred for DSP application and why? **7**

b) Explain what is meant by instruction pipelining? A non-pipelined system takes 100ns to process a task. The same task can be performed in 4 segments pipelined into 20ns each. Determine speed up ratio of pipeline for 1000 tasks. **6**

OR

2. a) Draw basic block diagram of MAC unit and explain how convolution is performed using a single MAC unit? **7**

b) Distinguish between multiple access memory and multiported memory. **6**

3. a) Let the content of ARP, AR2 and INDX register be 2, 1250h and 2h respectively and contents of data memory location 1240h-1260h be filled with the data 2345h. Let SXM be 0. Find the value of ACC and AR2 after sequential execution of following instructions **7**

i) LACC *, 0 ii) LACC * -, 1 iii) LACC * -, 3

b) Explain the status register STI of TMS320C5X in detail. **7**

OR

4. a) Explain the architecture of DSP TMS320C5X **8**

b) Explain the status register STO of TMS320C5X in detail. **6**

5. a) Explain the following instructions LST, LAR, ADD, SUB, LMMR. **8**

b) Write the contents of memory locations after execution of LST # 0, 00h if DP = 8 of Fig (a). **5**

Before Instruction Execution

Data men 400h	3E00h
ST0	5E00h
ST1	09A0h

Fig. (a)

OR

6. a) Explain following instructions **8**

1) SUB 8Sh, 2 2) LACC * + , 0
3) MACD 4) MPY

b) Write the content of accumulator after execution of LACC *, 4 if SXM = 0 of fig. (b) **5**

Before Instruction Execution

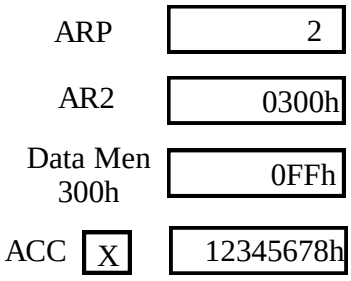

Fig. (b)

7. a) Draw and Explain central processing unit of C54X in detail. **7**

b) How many buses are there in C54X. Explain each in detail. **6**

OR

8. a) How Interrupts are handled in TMS320 C54X processor. Explain with flow chart. **7**

b) Explain following data addressing modes of C54X processor. **6**
1) Absolute 2) Accumulator 3) Stack

9. a) Compare the features of DSP processors C5X, C54X, C6X. **7**

b) Write steps of creating new project and building Assembly language code in CCS. **7**

OR

10. a) Give the brief introduction of Motorola DSP563XX processor. **7**

b) Draw the architecture of C6X and explain the working of central processing unit and data paths. **7**

11. a) Explain filtering of long data sequence using overlap and save method. **3**

b) Find the output y(n) of a filter whose impulse response is h(n) = {9 10} and input signal x (n) = {1 2 3 4 5 6 7 8} using overlap and add method. **10**

OR

12. Write short notes on **any three**. **13**

a) Interpolation filter b) Decimation filter
c) Wavelet filter d) Comparison of DFT and FFT time complexity.

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