

B.E. (Electronics Engineering / Elect. & Telecommunication / Elect. & Communication
Engineering) Seventh Semester (C.B.S.)

DSP Processor & Architecture

P. Pages : 2

Time : Three Hours



NRJ/KW/17/4582/4590

Max. Marks : 80

- Notes :
1. Solve Question 1 OR Questions No. 2.
 2. Solve Question 3 OR Questions No. 4.
 3. Solve Question 5 OR Questions No. 6.
 4. Solve Question 7 OR Questions No. 8.
 5. Solve Question 9 OR Questions No. 10.
 6. Solve Question 11 OR Questions No. 12.
 7. Assume suitable data whenever necessary.

1. a) Explain the difference between Von-Neumann and Harvard architecture for the computer. Which architecture is preferred for DSP applications and why? 7
 b) Define the following terms : 4
 i) Multiple access memory. ii) Multi ported memory.
 c) Explain why MAC operation is implemented in hardware in programmable DSPs. 2

OR
2. a) Explain what is meant by instruction pipelining. Explain with an example how pipelining increases the throughput efficiency. 8
 b) What is range of numbers that can be represented in a fixed point format using 16 bits, If the numbers are treated as 5
 a) Signed integers b) Signed fractions
3. a) What are the different buses of TMS320C5X and their functions. 5
 b) List the status register bits of 5X and their functions. 5
 c) What are features of a central arithmetic logic unit of TMS320C5X. 3

OR
4. a) Explain direct addressing mode and show with a diagram how 16 bit address is formed. 5
 b) Let the value of ARP, AR2 and INDX register be 2, 1250 h and 2h respectively and the content of the data memory location 1240h-1260h be filled with the data 2345h. Let SXM be 0. The value of ACC and AR2 after the following sequence of LACC (Load accumulator with shift) instructions are executed serially. 8
 LACC *, 0
 LACC *+, 1
 LACC *-, 2
 LACC *0+, 4
 LACC *0-, 3
5. a) Explain the following instructions LST, LAR, ADD, SUB, LMMR. 10

- b) Write the contents of memory locations after execution of LST # 0, 00h. if DP = 8. Before execution 4

Data Mem	3E00h
400h	
ST0	5E00h
ST1	09A0h

OR

6. a) Consider the following program involving only single word instructions: 7
- ADD * +
SAMB TREG 0
MPY * +
SQRA * +, AR 2

Show the table showing contents of instruction pipeline.

- b) Explain the block diagram of DSP starter kit. 7

7. a) Draw the block diagram of TMS320C54X and explain the following blocks. (Describe in brief the following blo) 10
- i) Arithmetic and logic unit ii) Accumulators
iii) Barrel shifter iv) CSSu
v) Address generation unit in brief.

- b) Explain TDM serial port with respect to TMS320C54X. 3

OR

8. a) Describe stack, accumulator and absolute addressing mode with respect to TMS320C54X. 6
- b) Write in brief about interrupts handling in TMS320C54XX. 7
9. a) Draw the architecture of TMS320C6X and explain the working of central processing unit and data paths. 8
- b) What is code composer studio? How to build project in CCS. 5

OR

10. a) Compare the features of DSP processors TMS320C5X, TMS320C54X, TMS320C6X. 6
- b) Draw an architecture of Motorola DSP563XX and explain in brief. 7

11. a) Describe overlap same and overlap add methods for filtering long data sequences. 8
- b) A time domain sequence of 73 elements is to convolved with another time domain sequence of 50 elements using DFT to transform the two sequences, multiplying them and taking IDFT to obtain resulting time domain sequence. DIT algorithm is used to take DFT and IDFT. Determine the total number of complex multiplications needed to implement the convolution. Assume that each butterfly computation requires one complex multiplication. 6

OR

12. Write short notes on **any three**. 14
- 1) Interpolation filter 2) Decimation filter 3) Wavelet filter
4) Comparison of DFT and FFT time complexity.
