

Faculty of Engineering & Technology
Eighth Semester B.E. (Electronics Engg./EDT)/
Eighth Semester B.E. Examination
DIGITAL SYSTEM DESIGN
Sections—A & B

Time—Three Hours]

[Maximum Marks—80

INSTRUCTIONS TO CANDIDATES

- (1) All questions carry marks as indicated.
- (2) Answer **THREE** questions from Section A and **THREE** questions from Section B.
- (3) Assume suitable data wherever necessary.
- (4) Illustrate your answers wherever necessary with the help of neat sketches.

SECTION—A

1. (a) What are the different modelling in VHDL ? Explain briefly with examples. 7
- (b) What are the differences between primary and secondary design units ? Explain in detail. 6
2. (a) Explain the statements : 8
 - (i) GENERATE
 - (ii) EXIT
 - (iii) LOOP
 - (iv) IF

Used in VDHL along with suitable examples.

- (b) What is meant by subprogram and explain in detail ? 6
- 3. (a) Explain transport and delays with sample waveforms. 6
- (b) Write a test bench to test the functionality of 16 to 1 multiplexer. 7
- (a) Write a VHDL code for Byte Adder circuit using GENERATE statement. 7
- (b) Write a VHDL code for D flip-flop with asynchronous reset. 6
- 5. (a) Write a VHDL code for priority encoder by using it-then-else statement. 6
- (b) Write a VHDL code for 4 bit barrel shifter. 7

SECTION-B

- 6. (a) Draw the state diagram for J-K flip-flop. Also write VHDL codes for J-K flip-flop. 7
- (b) Write a VHDL code for BCD to seven segment decoder. 6
- 7. Write a VHDL code to detect a sequence 1010 using melay machine (overlapping is allowed). Also write a test bench to test this design. 13
- 8. (a) What is the difference between Static and Dynamic Hazards ? 4
- (b) What is the role of synchronisers in Digital Logic Design ? 4

- (c) Compare ROM, PLA and PAL. 5
- 9. (a) Explain place, map and route process in detail. 6
- (b) Explain the structure and operation of FPGA. 7
- 10. Write short notes on (any **three**) :
 - (a) Critical races
 - (b) CPLD
 - (c) Clock Skew
 - (d) State Vector Encoding. 14

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