B.E. (Electronics Engineering / Elect.& Telecommunication / Elect.& Communication Engineering)
Seventh Semester (C.B.S.)

Advanced Digital System Design

P. Pages : 2 **NRT/KS/19/3530/3538**

Time : Three Hours * 0 2 4 2 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Diagrams and chemical equations should be given whenever necessary.
11. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Discuss the steps for design and implementation of Digital Circuits. **8**

b) Write note on the features & capabilities of an HDL. **5**

OR

2. a) What is meant by 'abstraction level' ? Explain various levels of abstraction in VHDL. **6**

b) Explain different design units used in VHDL with their syntax. **7**

3. a) What are Data types in VHDL ? Explain in details. **6**

b) Write VHDL code to design 16:1 Mux using 4:1 Mux as a component. **8**

OR

4. a) Discuss the different classes of VHDL objects. **6**

b) Write VHDL code for BCD to seven segment decoder using behavioural modeling style. **8**

5. a) What is a test bench ? Write a VHDL test bench to test 4:1 Mux. **5**

b) Write VHDL code to design 4:16 binary decoder using generate statement. **8**

OR

6. a) What is subprogram ? Explain 'functions' and 'Procedure' with their syntax. **8**

b) Write VHDL code to design NXM RAM memory using generics (assume suitable values for N and M) **5**

7. Write the difference between Moore and Mealy circuits. Design a overlapping sequence detector for sequence 1011 with Moore state machine and implement it with D flip-flop and write VHDL code for the same. **14**

OR

8. Design and write VHDL code for a candy vending machine controller with following specifications : **14**
Input $\rightarrow$ Rs_5, Rs_10, Rs_20, clk, Reset.
Output $\rightarrow$ Candy_out, Rs._5_out, Rs_10_out
If reset = '1', machine goes in initial state, Else user can give Multiple inputs but once the total input reaches beyond Rs_20 then machine should deliver a candy (i.e. Candy_out should be asserted) and the due amount if any should be given out and machine goes to initial state.

9. a) Write short note on 'power analysis' in FPGA based system. **6**

b) Explain the concept of synthesis ? Explain step by step process of synthesis. **7**

OR

10. Write short note on **any two.** **13**

i) Optimization of arithmetic expression.

ii) Partitioning for synthesis.

iii) Pipelining in VHDL.

11. a) Explain architecture of CPLD. **7**

b) Write a note on PAL, PLA. **6**

OR

12. a) Write VHDL code for 3-bit ALU. **5**

b) Write VHDL code to design 4x4 matrix keypad scanner. **8**

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