B.E. (Elect. & Telecommunication / Elect. Communication Engineering) Seventh Semester (C.B.S.)

Elective - I : VLSI Signal Processing

P. Pages : 2 **NJR/KS/18/4597**

Time : Three Hours Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Use of non programmable calculator is permitted.

1. a) Explain fine Grain Pipelining with the help of example. **7**

b) Explain pipelining & parallel processing for low power. **7**

OR

2. a) It is necessary to reduce the power consumption of a system by atleast 5 times using pipelining for threshold voltage of 0.4V and initial supply voltage of 5V, at what level should the system be pipelined? What is the supply voltage of pipelined system? **7**

b) Design a parallel system with L (level of parallel processing) = 3, n (iteration factor) = 3k where k = no. of clock cycle. **7**

3. a) What is retiming? Explain the method of retiming which uses Cutset in combination of Slowdown. **7**

b) With an example explain following: **6**
i) Retiming for clock period minimization.
ii) Retiming for register minimization.

OR

4. a) Draw a constraint graph & use it to determine if following system of inequalities has a solution and find a solution if one exits using Bellman – ford algorithm. **7**

$$\begin{cases} r_4 - r_3 \le -1 \\ r_3 - r_2 \le 2 \end{cases} \qquad \begin{cases} r_1 - r_2 \le 0, \\ r_3 - r_1 \le 5, \\ r_4 - r_1 \le 4, \end{cases}$$

b) Explain properties of retiming with an example. **6**

5. a) Describe how to design parallel processing architectures using unfolding. **7**

b) Show that unfolding preserves number of delays. **6**

OR

6. a) Explain application of unfolding in **7**
i) Sample period Reduction
ii) Parallel processing.

b) Design word level processing using unfolding. **6**

7. a) Describe folding of Multirate systems. **7**

b) What is the significance of life time analysis for register minimization. **6**

OR

8. a) Explain folding algorithm with an example. **5**

b) Consider a DSP program that performs transpose operation of 3x3 matrix shown below. Find **8**
a) Life time analysis
b) Data Allocation using forward backward method.
c) Register minimization.
The matrix is

$$\begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$$

9. a) Construct a 2x2 convolution algorithm using Cook Toom algorithm with $\beta = 0, 1, 2$. **7**

b) Explain steps of modified Cook Toom algorithm. **6**

OR

10. Construct a 2x3 convolution algorithm using modified Winograd algorithm with $m(p) = p\,(p-1)\,(p+1)$ **13**

11. Construct a 4x4 cyclic convolution algorithm using CRT with $m(p) = p^4 - 1 = (p-1)\,(p+1)\,(p^2+1)$ **14**

OR

12. a) Construct a 3x3 fast convolution algorithm using inspection method. **7**

b) Explain Iterated convolution. Procedure for fast convolution. **7**

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