B.E. (Elect. & Telecommunication / Elect. & Communication Engineering)
Eighth Semester (C.B.S.)

Elective - III : CMOS VLSI Design

P. Pages : 2 **NJR/KS/18/4708**

Time : Three Hours * 0 7 0 4 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.
11. Use of non programmable calculator is permitted.

1. a) Explain the operation of NMOS enhancement transistor. **7**

b) Explain the following terms : **6**

i) Body effect

ii) Channel length modulation

iii) Drain punch through

OR

2. a) Derive the basic DC equations of MOS transistor in three regions of operation. **6**

b) Calculate the threshold voltage V_{TO} at $V_{SB} = 0$ for a polysilicon gate n channel MOS transistor with following parameters : Substrate doping density $N_A = 10^{16} / cm^3$, polysilicon gate doping density $N_D = 2 \times 10^{20} / cm^3$, Gate oxide thickness $t_{ox} = 500 A^o$, oxide interface fixed charge density $N_{OX} = 4 \times 10^{10} / cm^2$. **7**

3. Explain the five regions of operation of CMOS inverter DC transfer characteristics. Hence derive the expressions for the same. **14**

OR

4. a) Consider a CMOS inverter circuit with the following parameters : **8**

$V_{DD} = 3.3 V$, $V_{to,n} = 0.6 V$, $V_{to,p} = -0.7 V$, $K_n = 200 \mu A / V^2$, $K_p = 80 \mu A / V^2$

Calculate the noise margins of the circuit. The CMOS inverter being considered here has $KR = 2.5$ and $V_{to,n} \neq |V_{to,p}|$.

b) Design 2 : 1 MUX and 4 : 1 MUX using CMOS Transmission gates. **6**

5. Implement the following functions using CMOS logic gates - **13**

i) $Z = \overline{A}B + A\overline{B}$

ii) $Z = \overline{(ABC) + D}$

iii) $Z = A\,(\text{Buffer})$

iv) $Z = \overline{(A \cdot B) + (C \cdot D)}$

OR

6. a) Explain the operation of CMOS positive edge triggered D Flip Flop. **7**

b) Explain the operation of DRAM cell. **6**

7. a) Derive the expression for static, dynamic and short circuit power dissipation and hence total power dissipation. **9**

b) Explain capacitance estimation of MOS device indicating accumulation, depletion and inversion region. **5**

OR

8. a) Explain switching characteristics of CMOS inverter and hence derive expression for rise time, fall time and delay time of a CMOS inverter. **9**

b) Write a short note on charge sharing. **5**

9. a) Draw stick diagram of **7**

i) CMOS inverter

ii) Two input NAND gate

b) Explain the phenomenon of Latch up in CMOS. How it is avoided. **6**

OR

10. Write short notes on **any three.** **13**

i) Clocking Strategies.

ii) Layout Design Rules.

iii) Domino logic.

iv) Transistor sizing.

11. a) State and explain different types of faults. **7**

b) What is DFT? Explain in detail. **6**

OR

12. Write short notes on **any two.** **13**

i) BIST

ii) JTAG

iii) Boundary Scan Technique.

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