9. (a) Explain addressing modes of µp 8085. 4

(b) Explain Architecture of 8085 in detail. 9

**OR**

10. (a) Explain the following instructions :

(i) STAX B

(ii) Push B

(iii) DAD rp

(iv) LXI H, address. 8

(b) Explain the following pins of µp 8085 :

(i) Ready

(ii) HOLD

(iii) HLDA. 5

11. (a) Write an assembly language program to arrange 10 bytes stored from 8000 H in descending order and store in memory locations starting from COOOH. 8

(b) Explain bit format of SIM and RIM instruction in 8085. 5

**OR**

12. (a) Draw timing diagram of instruction SHLD 5000 H. 6

(b) Explain hardware interrupt structure of µp 8085. 7



**NTK/KW/15/7333**

**Faculty of Engineering & Technology**

**Third Semester B.E. (Information Technology)**

**(C.B.S.) Examination**

**DIGITAL ELECTRONICS & FUNDAMENTAL OF MICROPROCESSOR**

**Paper—IV**

Time—Three Hours] [Maximum Marks—80

**INSTRUCTIONS TO CANDIDATES**

(1) All questions carry marks as indicated.

(2) Answer **SIX** questions.

(3) Assume suitable data wherever necessary.

(4) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) Convert the following :

(i) $(596432.896)_D = (\ ?\ )_B$

(ii) $(10110101.0101)_G = (\ ?\ )_B$

(iii) $(ABCD.EF)_H = (\ ?\ )_8$

(iv) $(7654.32)_8 = (\ ?\ )_D$ 8

(b) Draw NAND and EX-OR gates and write their truth tables. 5

**OR**

2. (a) Write short note on ASCII code. 5

(b) State law of complementation in boolean algebra. 2

(c) Simplify the following function using boolean algebra :

(i) $f(A, B, C) = ABC + AB\overline{C} + A\overline{B}$

(ii) $f(A, B, C, D) = ACD + \overline{A}CD + AB\overline{C} + ABC$

(iii) $f(A, B, C, D) = A\overline{B}C\overline{D} + \overline{A}B\overline{C}D + ABCD + \overline{A}\overline{B}C\overline{D}$ 6

3. (a) Simplify using K-map :

(i) $f(A, B, C, D) = \Sigma m(0, 4, 5, 8, 9, 12, 13, 15) + d(1, 6, 14)$

(ii) $f(A, B, C, D) = \pi M(0, 4, 7, 13, 15)$ 6

(b) Express given function in standard SOP and standard POS forms :

$f(W, X, Y, Z) = \overline{W}\overline{X}Z + WX\overline{Y}Z + WY\overline{Z}$. 6

(c) Explain Min and Max terms. 2

**OR**

4. (a) Simplify using K-map and implement using NAND gates only :

$f(A, B, C, D) = \Sigma m(0, 4, 6, 8, 10, 12, 14)$. 7

(b) By finding standard POS form of :

$f(A, B, C, D) = A\overline{B}C\overline{D} + AB\overline{C} + \overline{A}BCD + ACD$

Write truth table of the function. 7



5. (a) Explain working of BCD adder circuit. 7

(b) Implement following functions using suitable decoders and logic gates :

(i) $f_1(A, B, C) = \Sigma m(0, 2, 3, 6, 7)$

(ii) $f_2(A, B, C) = \Sigma m(1, 4, 5, 7)$. 6

**OR**

6. (a) Implement the given function using 8 : 1 MUX : $f(W, X, Y, Z) = \Pi M(0, 4, 7, 11, 12, 15)$. 7

(b) Design full subtractor circuit using logic gates. 6

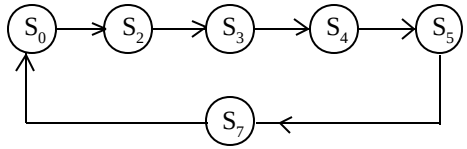
7. (a) Explain working of SR flip flop using NAND gates only. 6

(b) What is race around condition in JK flip flop ? 4

(c) What is difference between synchronous and asynchronous counters ? 4

**OR**

8. (a) Design Mod-6 synchronous counter using D flip flops. 8




(b) Convert the following :

(i) T to D flip flop

(ii) JK to SR flip flop. 6